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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,509	04/14/2004	Jonathan W. Byrn	03-2345/L13.12-0259	6456

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,509	BYRN ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 04/14/04; 06/08/05; 10/27/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 04/14/2004. Claims 1-20 are pending.

Claim Objections

Claim 1 is objected to because the recited "characteristics of the IP" (in step a) and the recited " characteristics of the IC" (in step b) need to be clarified. Appropriate correction is required.

Claim 2 is objected to because the recited "acceptable characteristics" does not clearly referred to which "characteristics" in claim 1, the "characteristics of the IP" (in claim 1, step b) or "characteristics of the IC" (in claim 1, step c). Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by **Chang et al. (US Patent No 6725432).**

Referring to claim 1 and similarly recited claim 11, Chang et al. disclose a process for characterizing intellectual property (IP) defining a circuit for integration at an anchor point in a context pre-defined IC, comprising steps of:

a) selecting a constraint on modification of each of a plurality of bounding constraint characteristics of the IP (*in col. 8, ll. 43 - col. 9, ll. 19 and in Fig. 1, Chang et al. disclose a step of selecting design criteria and inter-dependent design constraint of pre-designed circuit block or " IP" block);*

b) defining bounding constraints for each of the characteristics of the IP based on characteristics of the IC (*in col. 8, ll. 43-col. 9, ll. 19 and in Fig. 1, Chang et al. disclose a step of defining the bounding constraints of pre-designed circuit blocks, which include delay, routability, area, power dissipation, and timing, based on the design criteria of an ASIC (see " ASIC" in col. 8 , ll. 10-14);*

c) physical synthesizing the IP using the bounding constraints (*in col.25, ll.* 7-31, *Chang et al. disclose a step of synthesizing the circuit block based on the constraints. Also, the applicants admitted, " physical synthesis step is a standard physical synthesis of the RTL well known in the art"(specification, page 9, ll. 21-23)*);

d) testing the characteristics of the synthesized IP (*in col. 9, ll. 45-67, Chang et al. disclose a step of testing the synthesized circuit blocks to meet the design requirements*); and

e) iteratively repeating steps b), c) and d) using the test results to modify the bounding constraints for characteristics within the respective constraints of

modification until the characteristics of the IP are optimized (*in col. 8, ll. 54-col. 9, ll. 19 ; in Fig. 1 and Fig. 8, Chang et al. disclose a step of identifying and adjusting one constraint at a time, which include routability, area, power dissipation, and timing, of the pre-designed circuit blocks ("IP" blocks). One constraint is considered and adjusted at a time until it meets the overall design criteria).*

Referring to claim 2 and similarly recited claim 12, Chang et al. disclose the process of claim 1, wherein step (e) further comprises:

repeating steps (b), (c) and (d) through a range of acceptable characteristics, and selecting a set of characteristics from the range (*in col. 8, ll. 54-col. 9, ll. 19 ; in Fig. 1 and Fig. 8, Chang et al. disclose a step of identifying and adjusting one constraint at a time in a range of characteristics of the pre-designed circuit blocks ("IP" blocks): routability, area, power dissipation, and timing . One constraint is considered and adjusted at a time until it meets the overall design criteria).*

Referring to claim 3 and similarly recited claim 13, Chang et al. disclose the process of claim 2, further comprising:

identifying a plurality of anchor points in the platform, and

repeating steps (b)-(e) for each anchor point (*in col. 8, ll. 43 - col. 9, ll. 19; Fig. 1 and Fig. 8, Chang et al. disclose a step of identifying and adjusting inter-dependent design constraints of circuit blocked ("IP" blocks) in the chip planning design stage wherein the selected inter-dependent design constraints of each pre-designed circuit block depends on its adjacent circuit blocks. In other word, depending on where is the selected pre-designed circuit block is partitioned in the platform, the inter- dependent*

design constraints of each selected pre-design circuit block is generated, modified or adjusted repeatedly/until the overall design criteria are met).

Referring to claim 4 and similarly recited claim 14, Chang et al. disclose the process of claim 3, wherein the constraint on modification of each bounding constraint characteristic is selected from the group comprising fixed, variable and priority relationship (*in col. 8, ll. 54-67, Chang et al. disclose the constraints selected to be adjusted include delays, routability/ congestion, area, power dissipation, and timing. Depending on the design requirements or needs, the constraint characteristics can be a fixed, variable or prior parameters related to each other).*

Referring to claim 5 and similarly recited claim 15, Chang et al. disclose the process of claim 2, wherein the constraint on modification of each bounding constraint characteristic is selected from the group comprising fixed, variable and priority relationship (*in col. 8, ll. 54-67, Chang et al. disclose the constraints selected to be adjusted include delays, routability/ congestion, area, power dissipation, and timing. Depending on the design requirements or needs, the constraint characteristics can be fixed, variable, and/ or prior parameters related to each other).*

Referring to claim 6 **and similarly recited claim 16**, Chang et al. disclose the process of claim 2, further comprising:

f) storing the characteristics of the IP (*in col. 8, ll. 43-col. 9, ll. 19 and in Fig. 1, Chang et al. disclose the front-end acceptance design and the Chip planning design stages in which the characteristics of the pre-designed circuit bocks are used for adjusting the constraints. During the constraint adjusting process, the processed data*

which include the characteristic data of the pre-design circuit blocks must be stored for the processing).

Referring to claim 7 **and similarly recited claim 17**, Chang et al. disclose the process of claim 1, further comprising:

f) storing the characteristics of the IP (*in col. 8, ll. 43-col. 9, ll. 19 and in Fig. 1, Chang et al. disclose the front-end acceptance design and the Chip planning design stages in which the characteristics of the pre-designed circuit bocks are used for adjusting the constraints. During the constraint adjusting process, the processed data which include the characteristic data of the pre-design circuit blocks must be stored for the processing).*

Referring to claim 8 **and similarly recited claim 18**, Chang et al. disclose the process of claim 1, wherein the constraint on modification of each bounding constraint characteristic is selected from the group comprising fixed, variable and priority relationship (*in col. 8, ll. 54-67, Chang et al. disclose the constraints selected to be adjusted include delays, routability/ congestion, area, power dissipation, and timing. Depending on the design requirements or needs, the constraint characteristics can be fixed, variable, and/ or prior parameters related to each other).*

Referring to claim 9 **and similarly recited claim 19**, Chang et al. disclose the process of claim 1, further comprising:

identifying a plurality of anchor points in the platform, and

repeating steps (b)-(e) for each anchor point *(in col. 8, ll. 43 - col. 9, ll. 19; Fig. 1 and Fig. 8, Chang et al. disclose a step of identifying and adjusting inter-dependent*

design constraints of circuit blocked ("IP" blocks) in the chip planning design stage wherein the selected inter-dependent design constraints of each pre-designed circuit block depends on its adjacent circuit blocks. In other word, depending on where is the selected pre-designed circuit block is partitioned in the platform, the inter- dependent design constraints of each selected pre-design circuit block is generated, modified or adjusted repeatedly/until the overall design criteria are met).

Referring to claim 10 and similarly recited claim 20, Chang et al. disclose the process of claim 9, wherein the constraint on modification of each bounding constraint characteristic is selected from the group comprising fixed, variable and priority relationship (*in col. 8, ll. 54-67, Chang et al. disclose the constraints selected to be adjusted include delays, routability/ congestion, area, power dissipation, and timing. Depending on the design requirements or needs, the constraint characteristics can be fixed, variable, and/or prior parameters related to each other).*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
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VUTHE SIEK
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